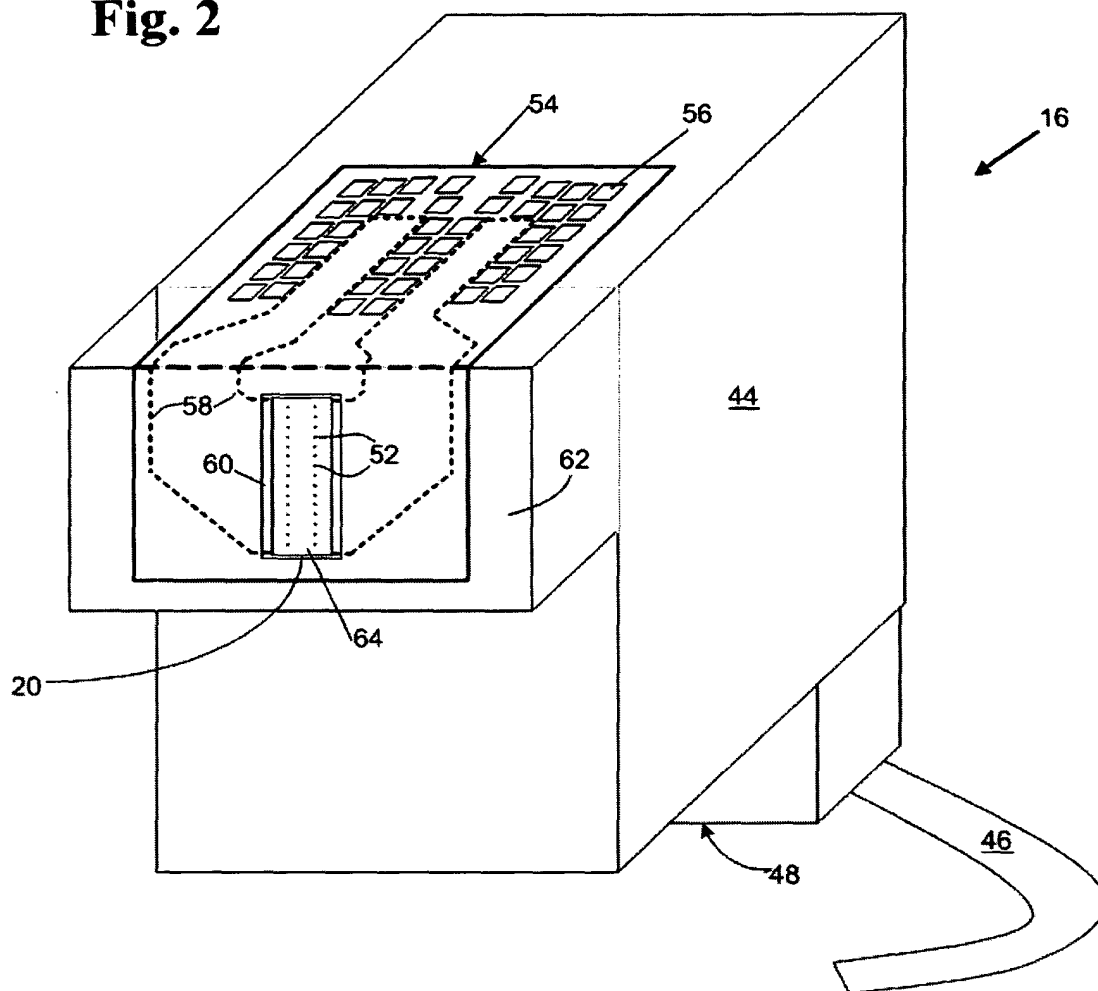
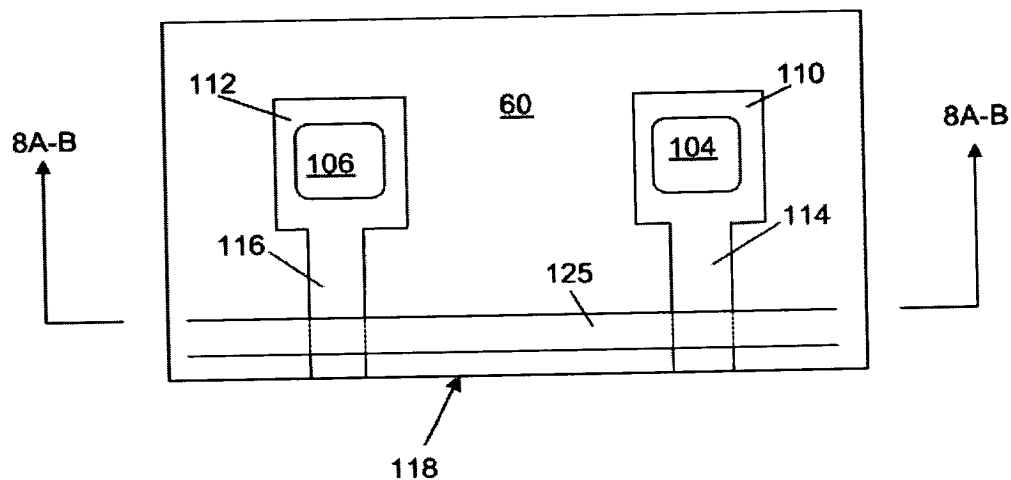
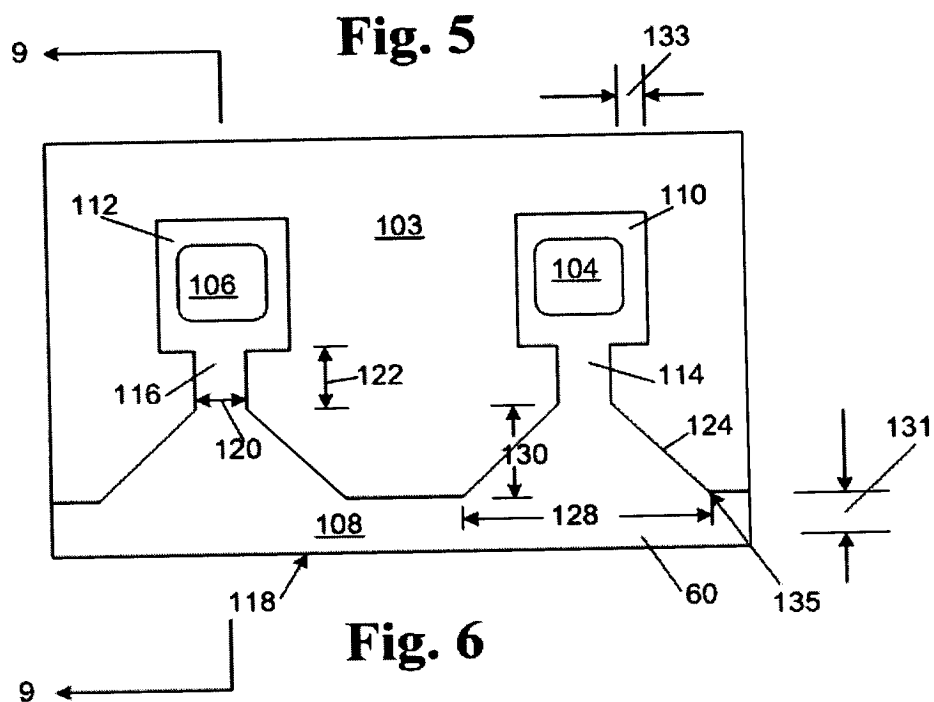


Fig. 2





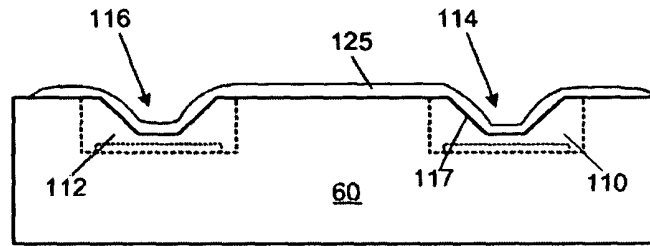


Fig. 8A

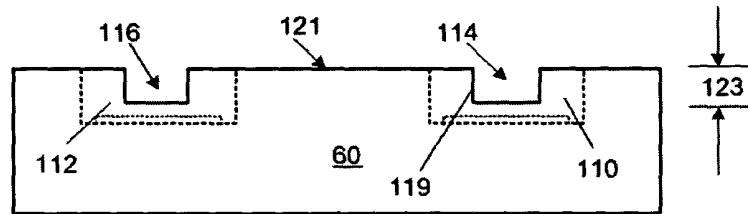


Fig. 8B

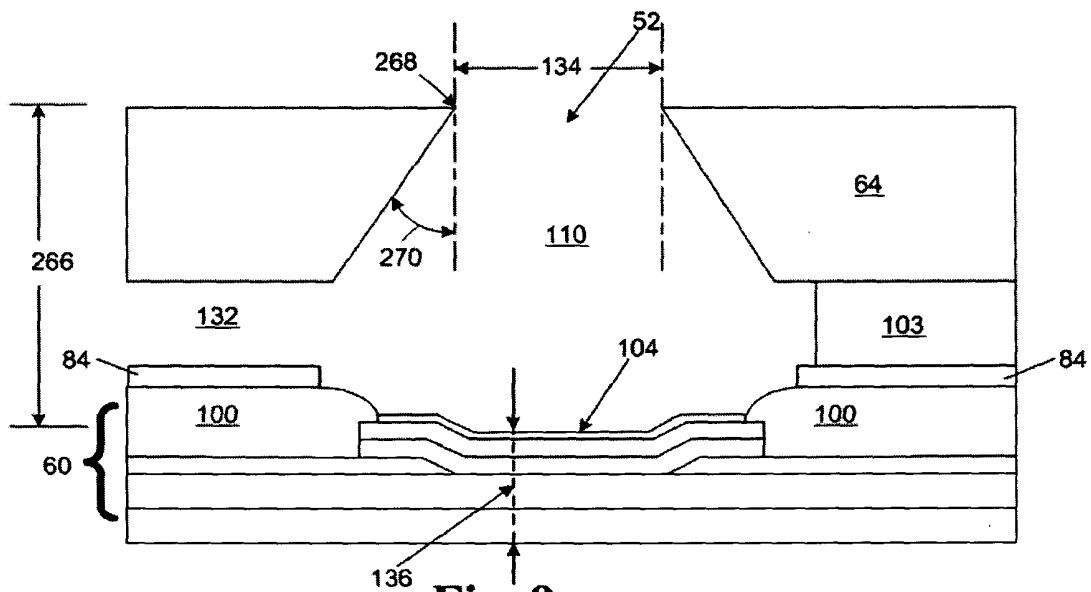


Fig. 9

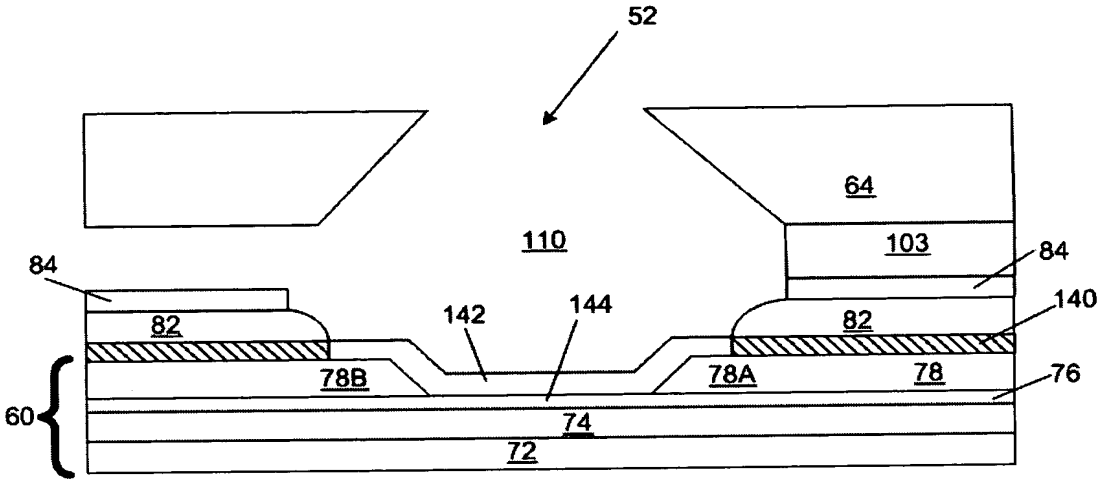


Fig. 10

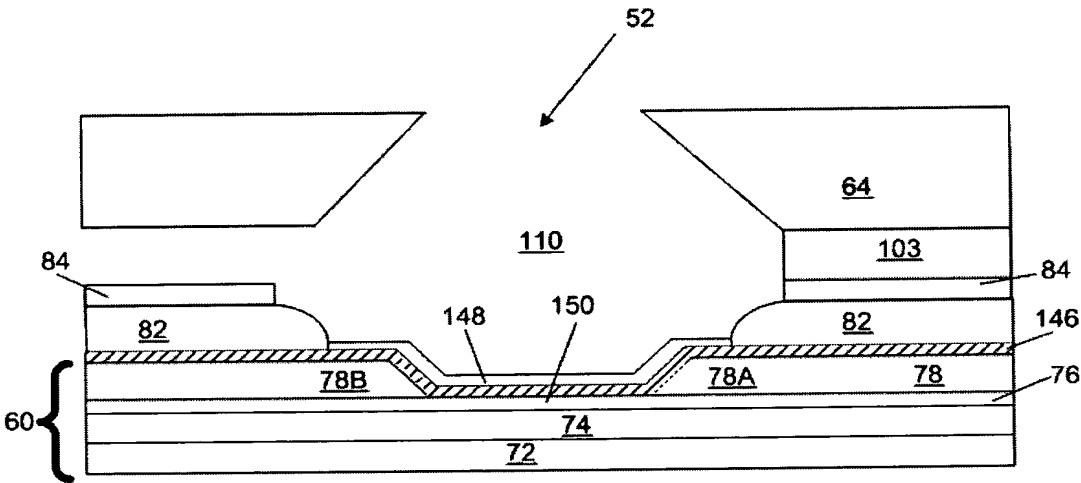


Fig. 11

A cross-sectional view of a semiconductor device. A substrate 60 is shown at the bottom. Two gates, 106 and 104, are formed on the substrate. Gate 106 is on the left and gate 104 is on the right. They are separated by a channel region 108. The gates are formed on a layer 103. The top surface of the gates is labeled 112 for gate 106 and 110 for gate 104. The side surfaces of the gates are labeled 116 for gate 106 and 114 for gate 104. A dashed line 142 is shown above the gates. An arrow 118 points to the substrate 60.

Fig. 13

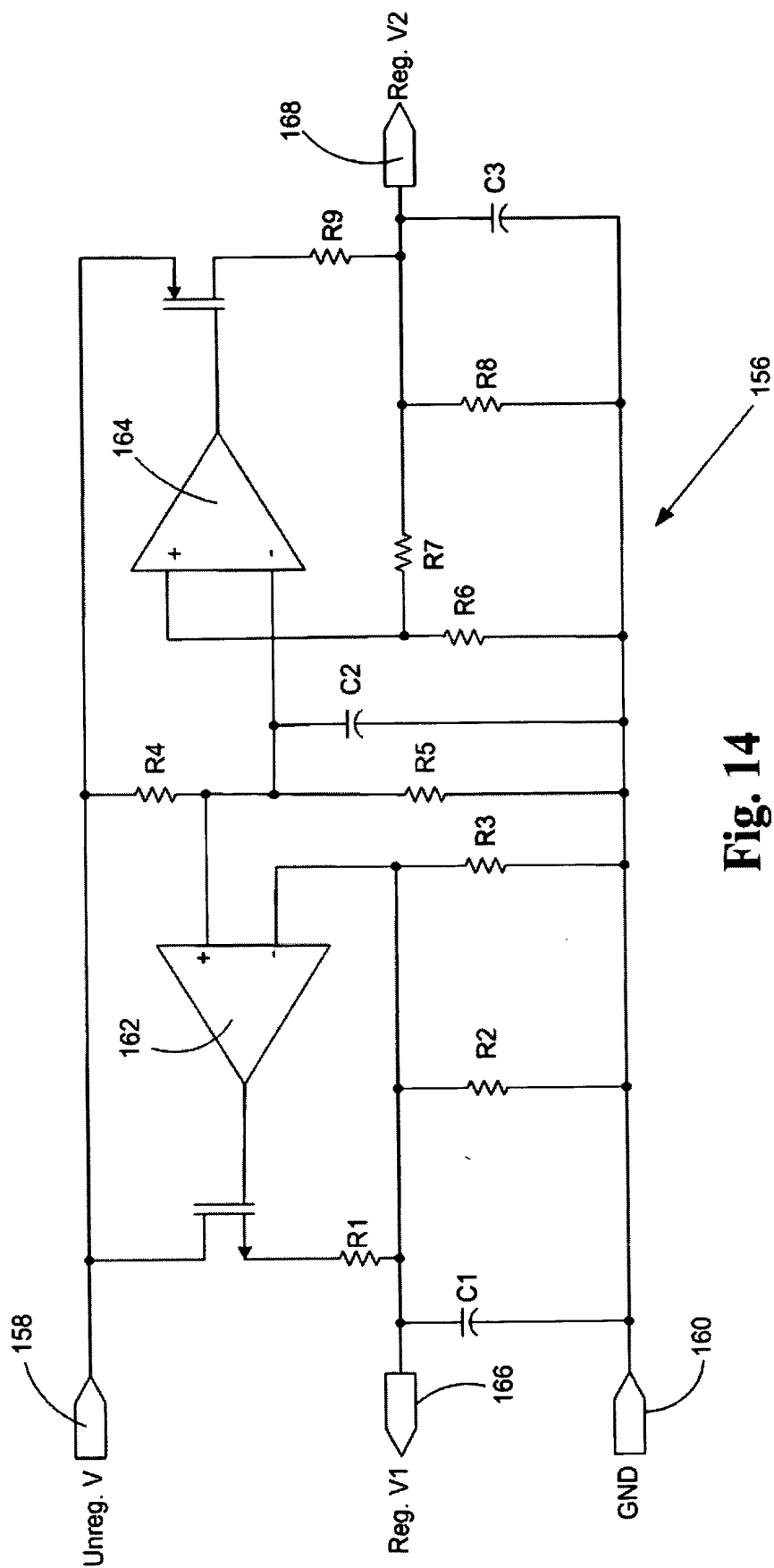


Fig. 14

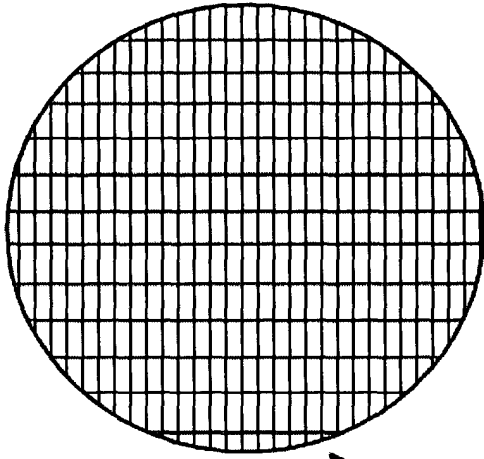


Fig. 15

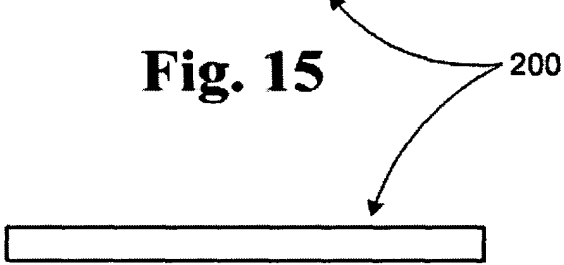


Fig. 16

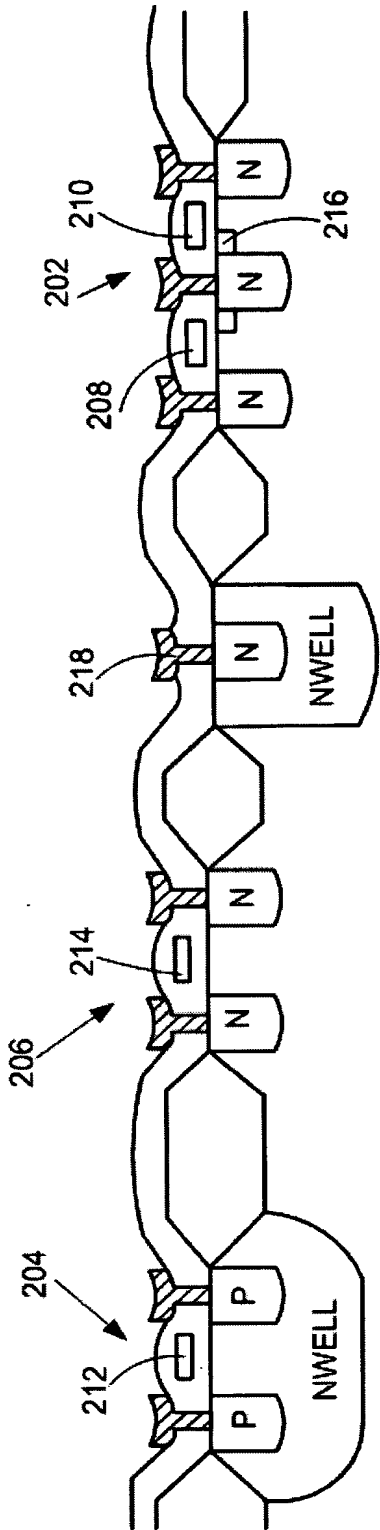


Fig. 17

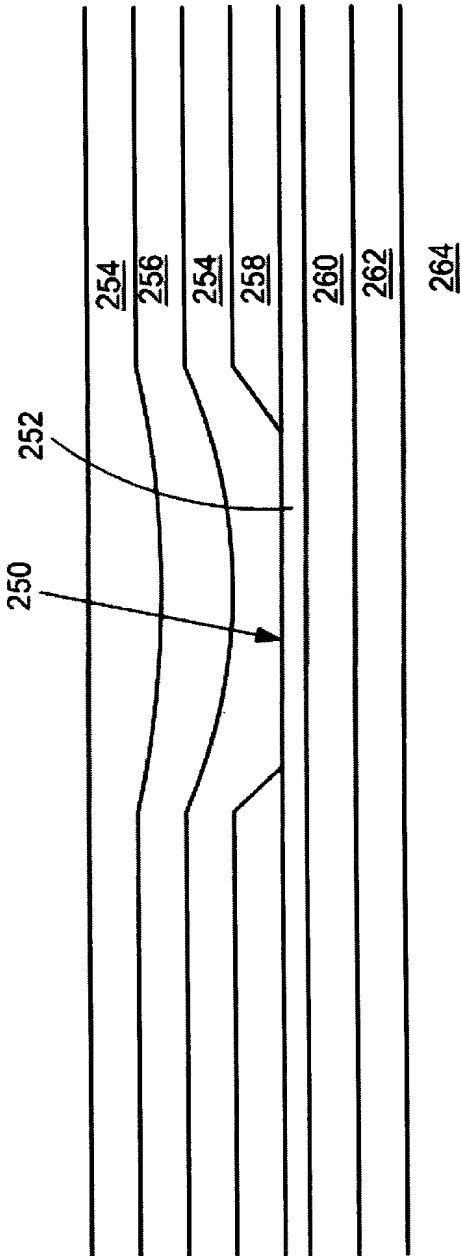


Fig. 18